Abstract

The present invention embodiment comprises an arrangement of integrated circuits with a UART device that is configurable to operate in a power-reduced mode while the clock frequency of serial data communication remains constant. In one example embodiment, an arrangement of a plurality of integrated circuit devices includes a first integrated circuit device driven by a first clock signal at a first clock rate. The arrangement contains a parallel data bus coupled to communicate with the first integrated circuit device in response to the first clock signal. The arrangement also includes a universal asynchronous receiver/transmitter (UART) chip with a serial communication circuit adapted to communicate serial data at a second rate defined by a second clock signal. The UART chip also encompasses a parallel bus interface circuit responsive to the first clock signal and adapted to pass data between the parallel data bus and the serial communication circuit. The UART chip also houses a data-storage-register circuit adapted to output status data to the parallel data bus, the status data being indicative of states of at least one of the serial communication circuit and the parallel bus interface circuit. The arrangement of integrated circuit devices further includes a clock control circuit adapted to reduce the first clock rate in response to a clock control signal. By reducing the first clock rate, the UART chip is configured to operate in a power-reduced mode while the serial communication circuit concurrently communicates serial data at the second rate.